ABSTRACT OF THE DISCLOSURE

A clock multiplier capable of modulating the duty cycle of the output clock comprises a first clock multiplication circuit, an inverter, a first low pass filter, a second low pass filter and an amplifier, the first multiplication clock being operative to multiply the frequency of an input clock, the inverter being operative to invert the input clock, the first low pass filter receiving the output clock of the inverter for being charged or discharged, the second low pass filter receiving the output clock of the first clock multiplication circuit for being charged or discharged, the amplifier being operative to compare the output voltages of the first low pass filter and the second low pass filter to perform a feedback control, so as to modulate the duty cycle of the output clock of the first multiplication clock to approach 50%.